IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An increasing ~~monotonous~~ monotonic counter over n bits formed as an integrated circuit, comprising:

an assembly of 2^{n+1}-(n+2) irreversible counting cells ~~(11, 11'; 11")~~ distributed in at least n groups of 2^p-1 counting cells, where p designates the group rank; and

at least n-1 parity calculators ~~(40)~~, each calculator providing a bit of rank p, increasing from the most significant bit of the result count, taking into account the states of the cells of the group of same rank.

2. (Original) The counter of claim 1, wherein the most significant bit is directly provided by the single cell of the group of rank 1.

3. (Original) The counter of claim 1, comprising n calculators, the most significant bit being provided by the calculator taking into account the state of the single counting cell of the group of rank 1.

4. (Currently Amended) The counter of claim 1, wherein each counting cell is formed of a one-time programming memory cell ~~(11, 11'; 11")~~, a ~~memorization~~ storage element of which is formed of at least one polysilicon resistor ~~(Rp; Rp1, Rp2)~~, programmable by irreversible decrease in its value.

5. (Currently Amended) A method for controlling the counter of claim 1, ~~consisting of~~ comprising causing a programming of a counting cell of a group of lower rank each time the parity controller of a group of immediately higher rank detects a parity.

6. (Original) The method of claim 5, implemented by a state machine in wired logic.

7. (Original) The method of claim 5, implemented by a microcontroller.